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10SCS31

Third Semester M.Tech. Degree Examination, December 2012
Advances in VLSI Design and Algorithms

Time: 3 hrs.

Max. Marks:100

Note: Answer any FIVE full questions.

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| 1 | <ul style="list-style-type: none"> a. Explain the integrated circuit design techniques. (10 Marks) b. Why we need Ip based design? Mention the types of Ip's. (04 Marks) c. Explain the Ip – life cycle with the help of flow diagram. (06 Marks) |
| 2 | <ul style="list-style-type: none"> a. Explain the fabrication theory with respect to design rules and yield. (05 Marks) b. Explain in detail, SCMOS design rules. (08 Marks) c. What are the traditional sources of unreliability? (07 Marks) |
| 3 | <ul style="list-style-type: none"> a. Define setup time and hold time. (04 Marks) b. What is dynamic latch and explain latch operation. (10 Marks) c. What is quasi static latch? (06 Marks) |
| 4 | <ul style="list-style-type: none"> a. Design a two bit shift register, using a dynamic latch. (10 Marks) b. What is clock skew? What are the sources of clock skew? (06 Marks) c. Explain the clock generation, with the help of PLL block diagram. (04 Marks) |
| 5 | <ul style="list-style-type: none"> a. With a neat structure, explain the operation of carry look ahead adder. (10 Marks) b. Write the detail structure of Booth's multiplier and explain. (10 Marks) |
| 6 | <ul style="list-style-type: none"> a. Explain the architecture of high density memory system. (10 Marks) b. Explain PLA with the help of its architecture, circuit, layout and delay. (10 Marks) |
| 7 | <ul style="list-style-type: none"> a. Explain some basic concepts of hardware description languages. (10 Marks) b. What is pipelining? Define through put and latency with respect to pipelining. (10 Marks) |
| 8 | <ul style="list-style-type: none"> a. With the help of a block diagram, explain the GALS system. (10 Marks) b. Write a short notes on : <ul style="list-style-type: none"> i) Gate level simulation ii) Switch –level modeling. (10 Marks) |

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
 2. Any revealing of identification, appeal to evaluator and/or equations written eg. 42+8 = 50, will be treated as malpractice.

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